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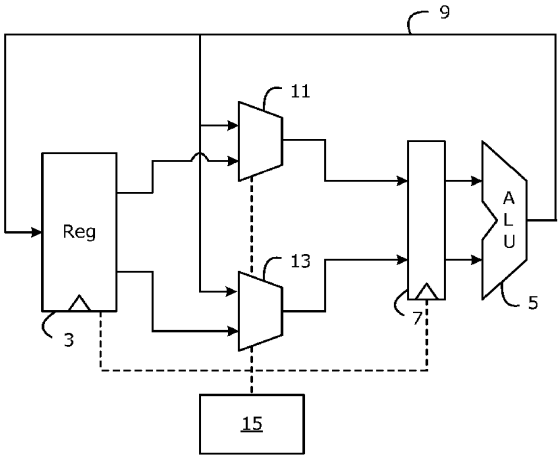
(54) Title: DATA PROCESSING METHOD AND APPARATUS



(57) Abstract: A data processing apparatus comprises a register file (3) connected to an ALU (5) via an ALU input register (7). A feedback path (9) is provided for storing results generated by the ALU (5) in the register file (3). A bypass circuit, for example comprising multiplexers (11 and 13), is provided for effectively bypassing the register file (3), thus allowing the results of the ALU (5) to be forwarded directly to the input register (7) of the ALU (5), so that the register file (3) can be bypasses when the result of a first instruction is used as the operand of a second instruction during a subsequent processing cycle. A bypass control means (15) is provided for determining when the result of a first instruction is only used once by a second instruction, and the timing of the first and second instructions is such that an operand for the second instruction is provided by the bypass network. When the bypass control means (15) determines this to be the case, the bypass control means (15) is further adapted to prevent the result of the first instruction to be written to the register file. In this case the contents will not be used in the future anymore. The invention has the advantage of saving power, by omitting this write to the register file.

WO 2007/057831 A1

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Data processing method and apparatus

The invention relates to a data processing method and apparatus, and in particular to a data processing method and apparatus having power reduction in register based instruction sets.

The invention further relates to a device, such as a mobile phone, PDA or alike, comprising such data processing apparatus.

In many Central Processing Units (CPUs), registers are used as fast local storage elements. Instructions operate on these registers by reading the operands from the registers and writing the result to a register. The provision of local registers means that fewer accesses are required to the main system memory to retrieve operands and to store results of ALU operations, which is considerably slower than accessing data from local memory.

Fig. 1 shows an example of a simplified data path in a typical pipeline data processing system 1. The data path comprises a register file 3, an Arithmetic logic Unit (ALU) 5, and an ALU input register 7. It is noted that references in the description of the background art and the description of the invention to a "register file" in the singular form can be interchanged with references to a "register" or "registers" in the plural form.

During a read register stage (RR), operands are read from the register file 3 and written to the ALU input register 7. In an execution stage (EXE) the calculation is done. In the next cycle the result is written (WR) to the register file 3 using the feedback loop 9.

Fig. 2 shows the operation of Fig. 1 when performing a simple instruction such as:

$$r2 = r0 + r1$$

whereby the contents of register r0 and r1 are added, and stored in register r2.

As shown in Fig. 2, during a first cycle t1 the instruction reads its operands from the register file 3 (i.e. it reads registers r0 and r1). The instruction is executed during cycle t2 by the ALU 5. The result is then stored in the register file 3 (i.e. in register r2) during cycle t3.

Fig. 3 shows the operation of such a simple data path in which two instructions are performed one after the other, whereby the second instruction is dependent on the result of the first instruction. For example, consider the operation of the following instructions:

r2 = r0 + r1, followed by

r4 = r2 + r3

As can be seen from Fig. 3, when the second instruction reads its operands, the first instruction is calculating the result, and so the second instruction cannot yet read the operand from the register r2.

This is explained further in Fig. 4. The second instruction cannot read (RR) its operands in cycle t2 because the first instruction is still calculating the result (EXE). The first instruction writes the result to the register r2 in cycle t3. Since the write (WR) takes place early in t3, this means that the second instruction can only validly read (RR) its operands asynchronously from register r2 (and register r3) in cycle t3, thus causing a delay in the data processing.

A known method of reducing this delay is to use a bypass network as shown in Fig. 5. In a similar manner to Fig. 1, the circuit shown in Fig. 5 comprises a register file 3 connected to an ALU 5, via an ALU input register 7, and having a feedback path 9 for storing results generated by the ALU 5 in the register file 3.

However, a bypass circuit comprising multiplexers 11 and 13 is also provided for effectively bypassing the register file 3. In other words, the multiplexers 11 and 13 enable the results of the ALU 5 to be forwarded directly to the input register 7 of the ALU 5, effectively bypassing the register file 3. The bypass circuit determines if the source register is the same as the destination register (in this case r2 and r2). If the source register matches the destination register, the bypass circuit is adapted to allow the ALU input register 7 to use the data from the multiplexers 11, 13, while the data is also being written to the register file 3.

In this way, the bypass circuit is adapted to pass an operation result of the first instruction to the second instruction as a source operand while the operation result is being written to the register file. It will therefore be appreciated that the second instruction can receive its source operand from the bypass circuit or the register file.

Fig. 6 shows how the second instruction is now able to read (RR) the operand data in cycle t2, i.e. via the bypass circuit, thus allowing instructions to be executed back-to-back. The provision of the bypass circuit enables the delay described in Figs. 3 and 4 to be removed, since the execution instruction (EXE) of instruction 2 can now take place in cycle t3. In other words, as the result is generated by the first instruction, it is bypassed in the same

cycle to the ALU input register 7, thus being available for execution by the second instruction.

The provision of a bypass circuit enables efficient utilization of the ALU generated data in a pipeline processor. However, the applicants have recognized that a pipeline processor having a bypass circuit has the disadvantage of utilizing more power.

The aim of the invention is to provide a data processing method and apparatus that enables power to be reduced in a data processing apparatus having a bypass circuit.

According to a first aspect of the invention, there is provided a data processing apparatus for processing first and second instructions in a pipelined manner. The data processing apparatus comprises a bypass circuit adapted to pass an operation result of the first instruction to the second instruction as a source operand while the operation result is being written to a register. The second instruction can receive its source operand from the bypass circuit or the register. The data processing apparatus further comprises write control means for selectively preventing the operation result of the first instruction from being written to the register.

Preferably, the write control means is adapted to determine when the operation result of the first instruction is only used once by another instruction and the timing of the first and second instructions is such that the source operand for the second instruction is provided by the bypass network, and for preventing the operation result from being written to the register accordingly.

The invention has the advantage of reducing power consumption, since a register write operation is avoided in certain circumstances.

According to a second aspect of the invention, there is provided a method of processing first and second instructions in a pipelined manner. The method comprises the steps of providing a bypass circuit for passing an operation result of the first instruction to the second instruction as a source operand while the operation result is being written to a register, wherein the second instruction can receive its source operand from the bypass circuit or the register. The method also comprises the step of selectively preventing the operation result of the first instruction from being written to the register.

According to a third aspect of the invention, there is provided an instruction for a data processing apparatus that processes first and second instructions in a pipelined manner, the data processing apparatus having a bypass circuit for passing an operation result

of a first instruction to a second instruction as a source operand while the operation result is being written to a register, wherein the second instruction can receive its source operand from the bypass circuit or the register. The instruction comprises a data bit for enabling the data processing apparatus to selectively prevent the operation result of the first instruction from being written to the register.

For a better understanding of the present invention, and to show more clearly how it may be carried into effect, reference will now be made, by way of example only, to the following drawings in which:

Fig. 1 shows an illustration of a simple data path in a pipeline processor;

Fig. 2 shows the timing sequence of the operation of Fig. 1;

Fig. 3 shows the operation of the simple data path of Fig. 1 when performing first and second instructions;

Fig. 4 shows the timing sequence relating to Fig. 3;

Fig. 5 shows an illustration of a simple data path in a pipeline processor having a bypass circuit;

Fig. 6 shows the timing sequence relating to the operation of Fig. 5;

Fig. 7 shows a data processing apparatus according to the present invention.

Fig. 7 shows a data processing apparatus according to the present invention. The data processing apparatus comprises a register file 3 connected to an ALU 5 via an ALU input register 7, and having a feedback path 9 for storing results generated by the ALU 5 in the register file 3. A bypass circuit, for example comprising multiplexers 11 and 13, is provided for effectively bypassing the register file 3. As mentioned above, the multiplexers 11 and 13 enable the results of the ALU 5 to be forwarded directly to the input register 7 of the ALU 5, thus effectively bypassing the register file 3.

In addition, a write control means 15 is provided, and is adapted to determine when the operation result of a first instruction is only used once by a second instruction, and the timing of the first and second instructions is such that a source operand for the second instruction is provided by the bypass network. When the write control means 15 determines this to be the case, the write control means 15 is further adapted to prevent the operation result of the first instruction from being written to the register file 3. In this case the contents

will not be used in the future anymore. Thus, it can be seen that the write control means 15 is adapted to selectively prevent the operation result from the first instruction from being written to the register file 3. The invention has the advantage of saving power, by omitting the write operation to the register file 3 during this special circumstance.

As can be seen from the above, a power saving can be achieved by the write control means 15 determining whether or not it can omit the write operation to the register file 3.

Preferably, this is achieved by including information in every instruction which enables the write control means 15 to determine if the write operation to the register file 3 can be prevented or omitted.

Preferably, a data bit is included in every instruction, which indicates if the write to the register file 3 may be omitted, or if the write to the register file 3 must be carried out. When this data bit is set an instruction can omit the write to the register file 3. When this data bit is not set the hardware must write to the register file 3. As will be appreciated by a person skilled in the art, other implementations are also possible for selectively preventing a write operation to be performed.

As mentioned above, the invention relies on the condition that the result of a first instruction is only used once by a second instruction, and the timing of the first and second instructions is such that an operand for the second instruction is provided by the bypass network.

In case of unexpected changes in program flow, such as caused by interrupts, the first and second instructions which were originally intended to be executed directly after each other are now separated by other instructions (i.e. from the interrupt handler).

In this case the write operation to the register file 3 is still needed because the second instruction cannot read its operands from the bypass network, but must fetch them from the register file 3.

Thus, in case of an unexpected change in program flow, the write control means 15 is adapted to ignore the data bit and always write to the register file 3 to allow the second instruction to read its operands from the register file 3 at a later time. In other words, the write control means 15 effectively overrides the decision that would otherwise prevent the operation result form being written to the register file 3.

This means of power saving can be applied to all CPUs which have a bypass network, including those which handle read after write (RAW) hazards.

As mentioned above, although the description refers to the data processing apparatus having a "register file" in the singular form, it is noted that this term is interchangeable with the term "register" or "registers". In other words, a reference to a register file can mean one or more registers, and vice versa.

While the invention has been described in the context of an "ADD" instruction, it will be appreciated that the invention can be used with any type of instruction, for which a bypass network is used to provide part of the operand(s).

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim, "a" or "an" does not exclude a plurality, and a single processor or other unit may fulfill the functions of several units recited in the claims. Any reference signs in the claims shall not be construed so as to limit their scope.

CLAIMS:

1. A data processing apparatus for processing first and second instructions in a pipelined manner, the data processing apparatus comprising:

- a bypass circuit adapted to pass an operation result of the first instruction to the second instruction as a source operand while the operation result is being written to a register, wherein the second instruction can receive its source operand from the bypass circuit or the register; and

- write control means for selectively preventing the operation result of the first instruction from being written to the register.

2. A data processing apparatus as claimed in claim 1, wherein the write control means is adapted to determine when the operation result of the first instruction is only used once by another instruction and the timing of the first and second instructions is such that the source operand for the second instruction is provided by the bypass network, and for preventing the operation result from being written to the register accordingly.

3. A data processing apparatus as claimed in claim 1 or 2, further comprising means for determining if there is an unexpected program flow, such that the first and second instructions are not operated upon in subsequent pipeline cycles.

4. A data processing apparatus as claimed in claim 3, wherein the write control means is adapted to write the operation result to the register, in the event that an unexpected program flow is determined.

5. A data processing apparatus as claimed in any one of claims 1 to 3, wherein the write control means is adapted to selectively prevent the operation result form being written to the register based on a data bit provided in the instruction.

6. A method of processing first and second instructions in a pipelined manner, the method comprising the steps of:

- providing a bypass circuit for passing an operation result of the first instruction to the second instruction as a source operand while the operation result is being written to a register, wherein the second instruction can receive its source operand from the bypass circuit or the register; and
- selectively preventing the operation result of the first instruction from being written to the register.

7. A method as claimed in claim 6, further comprising the step of determining when the operation result of the first instruction is only used once by another instruction and the timing of the first and second instructions is such that the source operand for the second instruction is provided by the bypass network, and for preventing the operation result from being written to the register accordingly.

8. A method as claimed in claim 6 or 7, further comprising the step of determining if there is an unexpected program flow, such that the first and second instructions are not operated upon in subsequent pipeline cycles.

9. A method as claimed in claim 8, further comprising the step overriding the preventing step, in the event that an unexpected program flow is determined.

10. A method as claimed in any one of claims 6 to 9, wherein the step of selectively preventing the operation result from being written to the register is based on a data bit provided in the instruction.

11. An instruction for a data processing apparatus that processes first and second instructions in a pipelined manner, the data processing apparatus having a bypass circuit for passing an operation result of a first instruction to a second instruction as a source operand while the operation result is being written to a register, wherein the second instruction can receive its source operand from the bypass circuit or the register, the instruction comprising:
- a data bit for enabling the data processing apparatus to selectively prevent the operation result of the first instruction from being written to the register.

12. Device comprising a data processing apparatus according to claims 1-5.

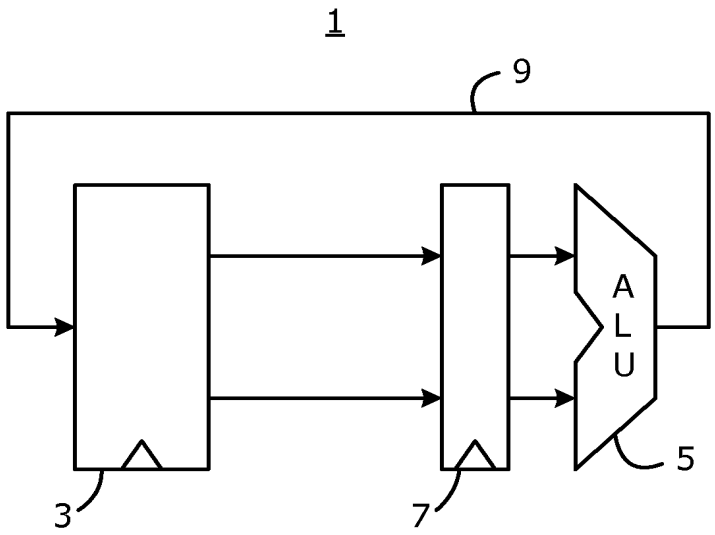

FIG. 1

	t1	t2	t3	t4	t5	t6
Instruction 1	RR	EXE	WR			

FIG. 2

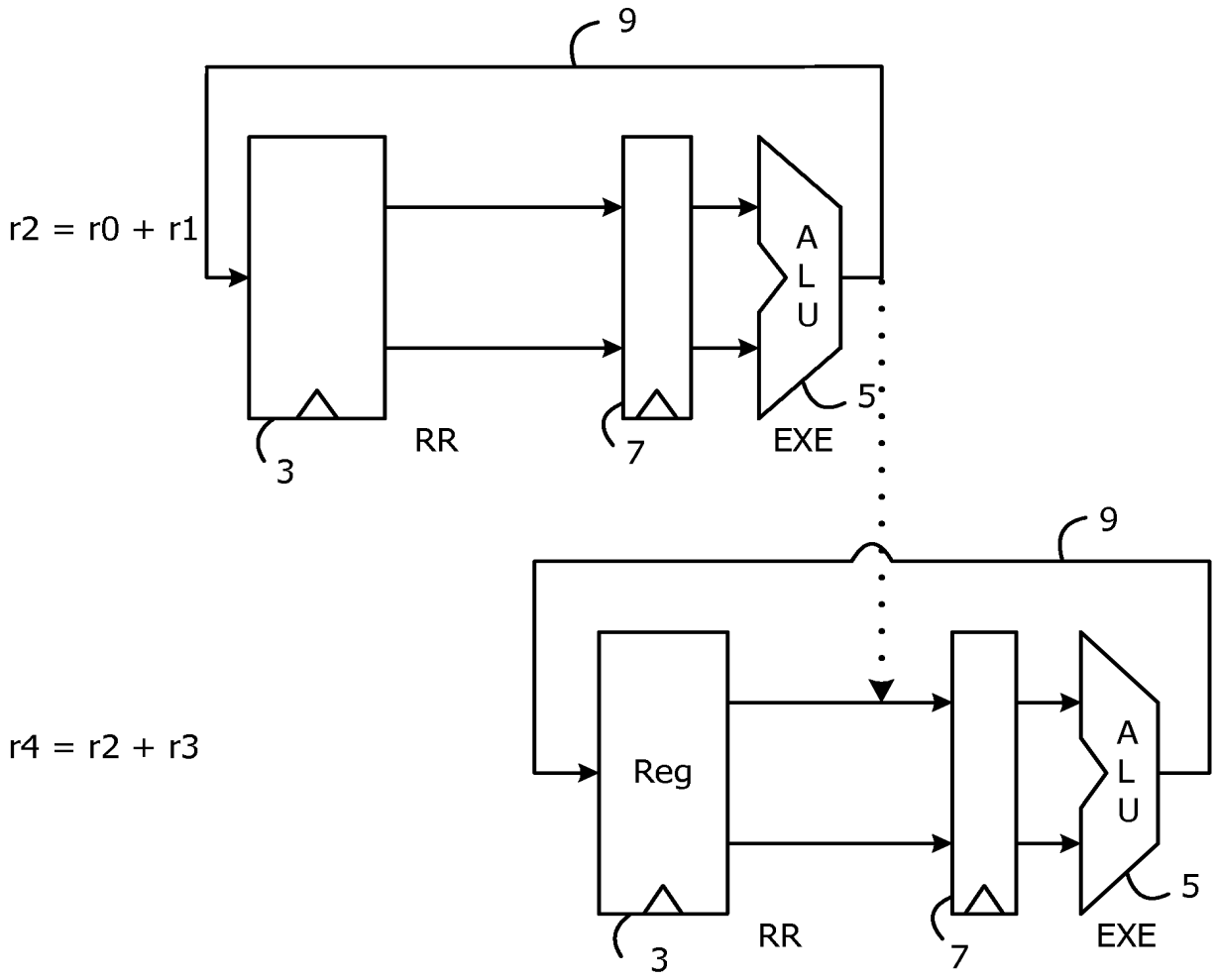

FIG. 3

	t1	t2	t3	t4	t5	t6
Instruction 1	RR	EXE	WR			
Instruction 2			RR	EXE	WR	

FIG. 4

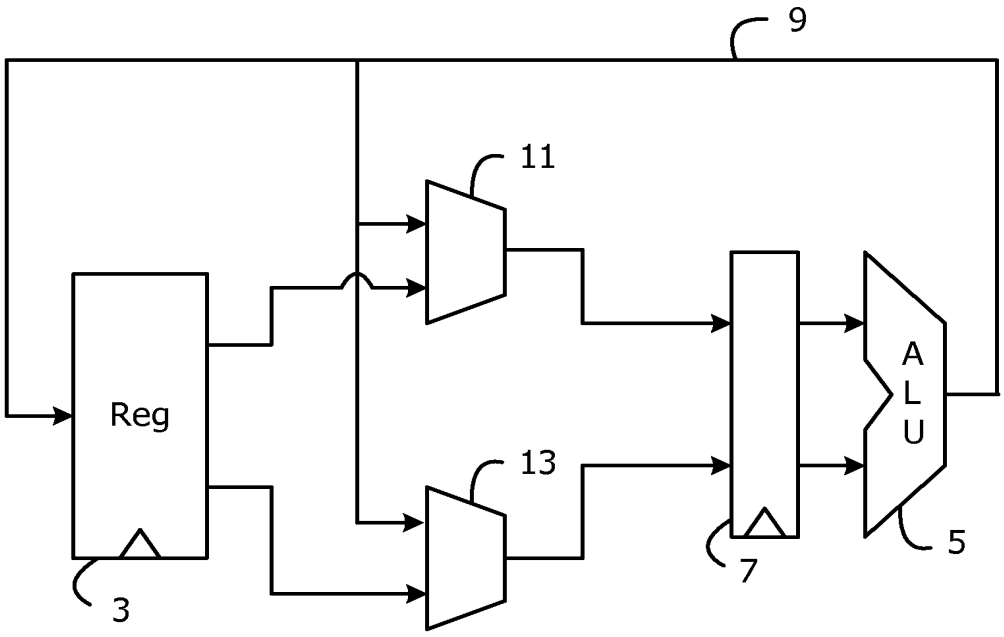

FIG. 5

	t1	t2	t3	t4	t5	t6
Instruction 1	RR	EXE	WR			
Instruction 2		RR	EXE	WR		

FIG. 6

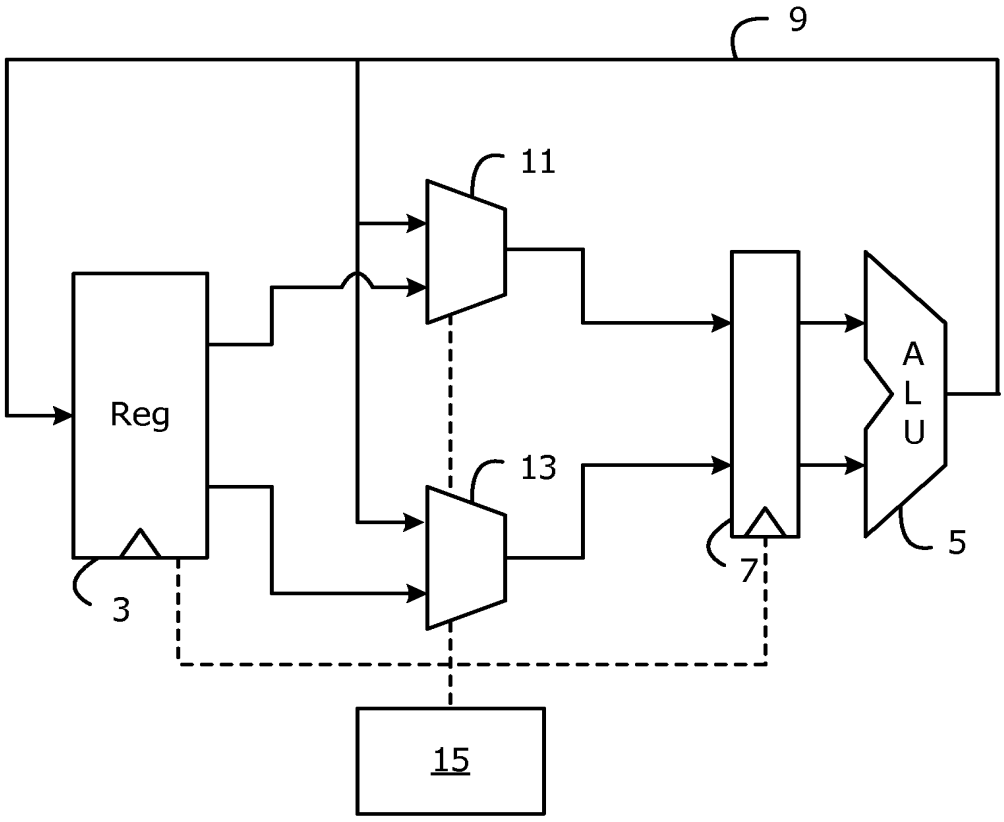

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/054213

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F9/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 199 629 A (ST MICROELECTRONICS SRL [IT]) 24 April 2002 (2002-04-24) paragraph [0017] - paragraph [0020] paragraph [0052] - paragraph [0054] paragraph [0057] - paragraph [0061] paragraph [0073] - paragraph [0074]	1-12
X	WO 01/61469 A2 (KONINKL PHILIPS ELECTRONICS NV [NL]) 23 August 2001 (2001-08-23) the whole document	1-12
X	WO 01/61478 A2 (KONINKL PHILIPS ELECTRONICS NV [NL]) 23 August 2001 (2001-08-23) the whole document	1,2,5-7, 10-12

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
2 March 2007	15/03/2007

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2006/054213

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